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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,713	04/14/2004	Jae-Bon Koo	61610123US	5231

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
10/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/823,713	KOO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-33* is/are pending in the application.

4a) Of the above claim(s) *5,7-10 and 13-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed August 16, 2007 has been entered; no new claims have been introduced.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. ("Yamazaki") USPN 6,506,635 in view of Kunii ("Kunii") JP 7-263705.

Yamazaki discloses (figs. 1-4 and col. 9, lines 56-65) a flat panel display, comprising: a pixel array portion 102 having a plurality of pixels arranged thereon; and a driving circuit portion 103 for driving the plurality of pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion comprising a plurality of channel regions 212 corresponding to multiple gates 206e and having a different resistance value than a thin film transistor in the driving circuit portion -- **note that regions 217 and 209 of the driving circuit are made of crystalline silicon while regions 212 of the pixel region are made of amorphous silicon having a lower field effect mobility than regions 217 and 209 indicating different resistance values**, but does not specifically disclose an offset region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel

region, a second source/drain region 52 contacting the second channel region, and an offset region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

Regarding claim 2, Yamazaki discloses in figs. 1-4 and 10-13 the pixel array portion and the driving circuit portion each having a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion -- note that regions 217 and 209 of the driving circuit are made of crystalline silicon while regions **212 of the pixel region are made of amorphous silicon** having a lower field effect mobility than regions 217 and 209 which **would mean a higher resistance value**.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Kunii.

Yamazaki discloses (figs. 1-4 and col. 9, lines 56-65) a flat panel display, comprising: a pixel array portion 102 having a plurality of pixels arranged thereon; and a driving circuit portion 103 for driving the plurality pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion comprising a plurality of channel regions 212 corresponding to multiple gates 206e and having a different resistance value in its gate region (channel region 212 under the gate) than a thin film transistor in the driving circuit portion -- **note that regions 217 and 209 of**

the driving circuit are made of crystalline silicon while regions 212 of the pixel region are made of amorphous silicon having a lower field effect mobility than regions 217 and 209 indicating different resistance values, but does not specifically disclose an offset region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel region, a second source/drain region 52 contacting the second channel region, and an offset region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Kunii as applied to claim 3 above and in further view of Shibata et al. ("Shibata") US PG-Pub 2005/0247940.

The combined references disclose the device structure as recited in the claim, but do not specifically disclose an offset region having a higher resistance than the thin film transistor in the driving circuit portion.

Shibata discloses in figs. 1-7 a flat panel display, comprising: a pixel array portion having a plurality of pixels arranged thereon; and a driving circuit portion for driving the plurality of pixels of the pixel array portion, and an offset region 104 being positioned directly between the

first channel region 101 and the second channel region 102, the offset region having a higher resistance than the thin film transistor in the driving circuit portion.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an offset region having a higher resistance than the thin film transistor in the driving circuit portion. The motivation would have been to yield a device with an increased on current as taught by Shibata (abstract and par. 159).

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Kunii.

Yamazaki discloses (figs. 1-4 and 7-13 and col. 9, lines 56-65) a flat panel display, comprising: a pixel array portion 102/1001(figs. 1 and 11) having a plurality of pixels arranged thereon; and a gate driving circuit portion 103/1002 and a data driving circuit portion 103/1003 for driving the plurality of pixels of the pixel array portion, wherein at least one thin film transistor in the pixel array portion comprising a plurality of channel regions 212 corresponding to multiple gates 206e and having a different resistance value from at least one thin film transistor of plurality of thin film transistors in the gate driving circuit portion and data driving circuit portion -- **note that regions 217 and 209 of the driving circuit are made of crystalline silicon while regions 212 of the pixel region are made of amorphous silicon having a lower field effect mobility than regions 217 and 209 indicating different resistance values**, but does not specifically disclose an offset region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel region, a second source/drain region 52 contacting the second channel region, and an offset

region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

Regarding claim 12, Kunii discloses the offset region 8 being positioned directly between the first channel region and the second channel region.

7. Claim 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. ("Sano") US PG-Pub 2003/00147018 in view of Kunii.

Sano discloses in figs. 2, 3 and 5 a flat panel display, comprising: a pixel array portion 100 having a plurality of pixels arranged thereon; and a driving circuit portion 101 for driving the plurality of pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion comprising a plurality of channel regions **C** corresponding to multiple gates **G** and having a different resistance value than a thin film transistor in the driving circuit portion -- **note that the smaller grains in the pixel portion contribute to high resistance value in thin film transistors in the pixel array portion indicating different resistance values (paragraphs 55 and 56)**, but does not specifically disclose an offset region directly contacting a first channel region and a second channel region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel region, a second source/drain region 52 contacting the second channel region, and an offset

region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Sano by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

Regarding claim 2, Kunii discloses the pixel array portion and the driving circuit portion each having a plurality of thin film transistors and where at least one thin film transistor of the plurality of thin film transistors in the pixel array portion has a resistance value higher than any of the plurality of thin film transistors in the driving circuit portion -- **note that the smaller grains in the pixel portion contribute to high resistance value in thin film transistors in the pixel array portion indicating different resistance values (paragraphs 55 and 56).**

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sano in view of Kunii.

Sano discloses in figs. 2,3 and 5 a flat panel display, comprising: a pixel array portion 100 having a plurality of pixels arranged thereon; and a driving circuit portion 101 for driving the plurality pixels of the pixel array portion, wherein a thin film transistor in the pixel array portion comprising a plurality of channel regions **C** corresponding to multiple gates **G** and having a different resistance value in its gate region than a thin film transistor in the driving circuit portion -- **note that the smaller grains in the pixel portion contribute to high resistance value in thin film transistors in the pixel array portion indicating different**

resistance values (paragraphs 55 and 56), but does not specifically disclose an offset region directly contacting a first channel region and a second channel region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel region, a second source/drain region 52 contacting the second channel region, and an offset region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Sano by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sano in view of Kunii as applied to claim 3 above and in further view of Shibata.

The combined references disclose the device structure as recited in the claim, but do not specifically disclose an offset region having a higher resistance than the thin film transistor in the driving circuit portion.

Shibata discloses in figs. 1-7 a flat panel display, comprising: a pixel array portion having a plurality of pixels arranged thereon; and a driving circuit portion for driving the plurality of pixels of the pixel array portion, and an offset region 104 being positioned directly between the first channel region 101 and the second channel region 102, the offset region having a higher resistance than the thin film transistor in the driving circuit portion.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an offset region having a higher resistance than the thin film transistor in the driving circuit portion. The motivation would have been to yield a device with an increased on current as taught by Shibata (abstract and par. 159).

10. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano in view of Kunii.

Sano discloses in figs. 2, 3 and 5 a flat panel display, comprising: a pixel array portion 100 having a plurality of pixels arranged thereon; and a gate driving circuit portion 120 and a data driving circuit portion 110 for driving the plurality of pixels of the pixel array portion, wherein at least one thin film transistor in the pixel array portion comprising a plurality of channel regions **C** corresponding to multiple gates **G** and having a different resistance value from at least one thin film transistor of plurality of thin film transistors in the gate driving circuit portion and data driving circuit portion -- -- **note that the smaller grains in the pixel portion contribute to high resistance value in thin film transistors in the pixel array portion indicating different resistance values (paragraphs 55 and 56),** but does not specifically disclose an offset region directly contacting a first channel region and a second channel region.

Kunii discloses in fig. 1 a plurality of channel regions comprising a first channel region 61 and a second channel region 62; a first source/drain region 51 contacting the first channel region, a second source/drain region 52 contacting the second channel region, and an offset region 8, and wherein the offset region directly contacts the first channel region and the second channel region and has a lower doping concentration than a doping concentration of the first source/drain region and a doping concentration of the second source/drain region.

Therefore, in view of Kunii's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Sano by incorporating an offset region. The motivation would have been to suppress a leak current as taught by Kunii.

Regarding claim 12, Kunii discloses the offset region 8 being positioned directly between the first channel region and the second channel region.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS
October 19, 2007

A. Sefer
Patent Examiner
Art Unit 2826